A 2.7V Image Reject Receiver for DECT

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Abstract-- An image reject receiver IC for DECT with min. 27dB power gain is presented. The effect of different realizations of phase shifter networks on the receiver performance is discussed in detail. It is shown that this kind of architecture gives a large gain in overall cost, because of the decrease of external components in the RF and IF path of the complete receiver.

I. Introduction

The need for cost reduction in digital cordless phones is primarily driven by the competition to very low cost analog environment. Therefore it is necessary to integrate as many expensive components as possible of the analog part of the telephone on an IC. The performance of the integrated circuits should give the possibility to use the lowest cost components even with the drawback of higher power consumption.

In this paper the realization of an image reject receiver is described, which helps to reduce the overall cost of the receiver by the reduction of external components and the possibility to drive a very low cost SAW-filter with less matching elements than before.

II. The Image Reject Receiver IC

The DECT image reject receiver is based on the second generation receiver IC, briefly discussed in [1]. It is manufactured in a 25GHz bipolar process. To reduce the overall cost and to achieve a higher integration level the LNA is integrated on the IC. In addition to this an external filter was made dispensable by image reject down mixing. Also an integrated bandpass filter replaces the external tank circuit for noise bandwith reduction in the limiter. This filter is realized by a second order operational amplifier bandpass filter.

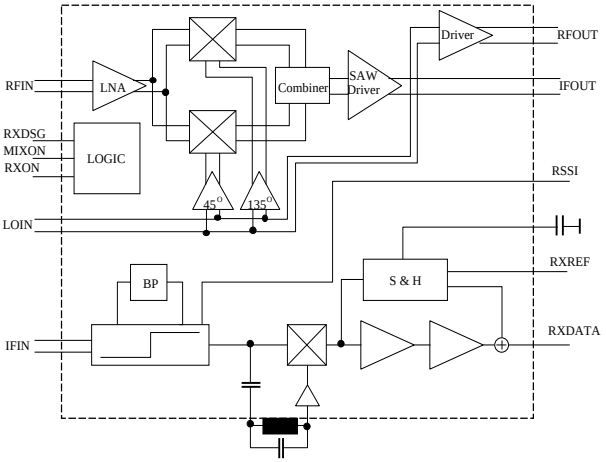

Fig. 1 Block Diagram of the Image Reject DECT Receiver

The receiver IC ist controlled by three logic signals delivered from the baseband or the transmitter IC. The incoming DECT RF signal is boosted by the internal LNA by 17dB and downconverted to an intermediate frequency of approximately 110MHz. After an additional

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amplification by a SAW driver amplifier it has a fully differential interface to an external SAW filter which is responsible for the channel selection. A high gain limiter amplifier follows in the signal path behind the filter which has an additional bandpass function for noise bandwith reduction, and it also delivers the radio signal strength information (RSSI) to the baseband IC. The level of the signal, which is now constant in amplitude after the limiter amplifier, is demodulated by a coincidence demodulator and converted to a digital output signal. An additional feature of this receiver IC is an integrated driver amplifier which is used in transmit mode to drive the power amplifier. The transmit signal is provided by the TX IC, and it can be also used as the local oscillator signal for the image reject down mixer. The driver amplifier is included on the RX IC to maximize the isolation between driver output and VCO. All signal interfaces are fully differential to minimize crosstalk. A block diagram of the complete receiver is shown in figure [1].

III. Circuit Description of the Image Reject Frontend

For the RF input of the IC a differential LNA has been choosen to minimize pin count and substrate coupling. The LNA is designed to have the maximum possible gain, to minimize the overall noise figure, and maximum linearity, to achieve the required overall DECT performance, which leads to a LNA power consumption of 32mW with a supply voltage of 2.7V.

The major task while designing an image reject front end is to find a good compromise between noise figure, linearity and image rejection. It is not useful to make a phaseshift at the RF frequency, because a phase shifter following the LNA will have a negative effect on the overall noise figure of the receiver. Which phase shifter networks should be used? A first order RC allpass structure has most probably the lowest loss of all passive phase shifter networks, but production spread will cause phase and amplitude errors. These errors will be much smaller in polyphase filters (for example [2]), but those phase shifters normally offer a higher loss. Therefore a combination of both, a polyphase combiner (see figure [2]), and a 1^{th} order allpass for LO phase shifting was choosen. The reason for this choice is simple: In the LO-path an amplitude error has no influence on the image rejection, because the signals are limited before they are fed to the Gilbert cell mixer's switching pairs. Too much loss in the LO path would worsen the noise performance of the receiver too much or would require a higher output level of the transmit IC. In the IF path the amplitude error has to be neglectable small, because every error will lower the achievable image rejection. The only drawback in this case is the high gain, the LNA and mixer has to deliver to get an neglectable influence of the combiner loss on the overall noise figure.

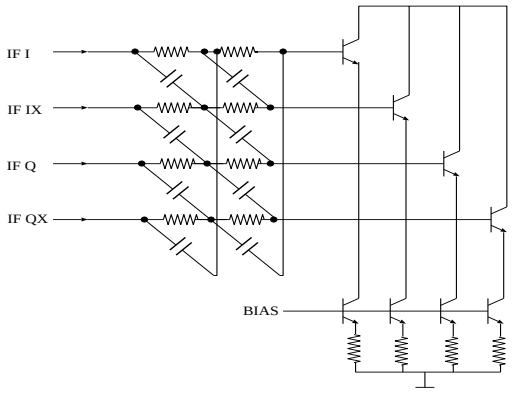

Fig. 2: Schematic of Polyphase Combiner

The major challenge in designing image reject receivers is to solve the linearity problems in the combiner. At this stage it is possible to have

a superposition of the wanted and the image signal. This effect defines the minimum linear range of the circuit. Especially at low supply voltages of 2.7V, or below, the available headroom of the circuits has to be used most efficient regarding temperature and technology spread.

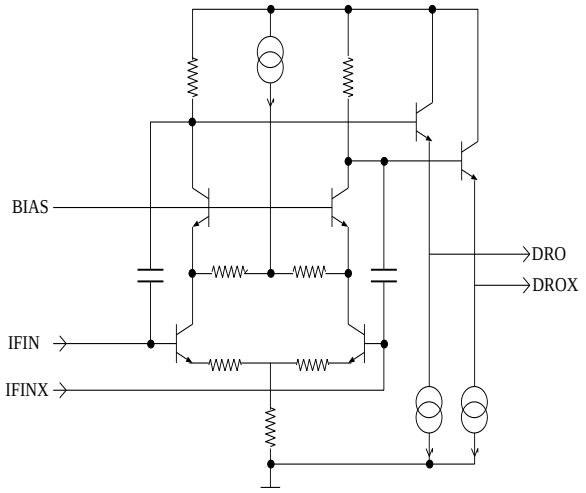

Fig. 3: Schematic of SAW Driver Amplifier

The combiner output directly goes to a high gain linear amplifier which drives the SAW filter by an emitter follower output to reduce the overall matching elements. To achive the high linearity in combination with a low noise figure it was necessary to have a large current in the differential amplifier driving the emitter followers (see figure [3]). To increase the output resistance of the differential pair in order to achieve more linearity at the common collector stages, with a moderate current, an additional current source was implemented. This current source takes over a large part of the DC current normally flowing through the output resitors of the differential pair. Therefore the output resitance can be increased. This results in a higher output resistance of the differential pair, making it easier to drive the output common collector stage

IV. Measurements

The image reject receiver IC is mounted in a TSSOP28 package. The overall current consumption of the complete receiver is approximately 51mA with a minimum supply voltage of 2.7V. 14mA are consumed in the intermediate frequency part of the IC. The image rejection of the front end was measured to be better than 38dBc for the complete DECT receive band. This value offers only a slight dependence on the LO input power. An input power of -10dBm is completely sufficient to achieve the best possible noise figure. The measurement results for the image rejection are presented in figure [4].

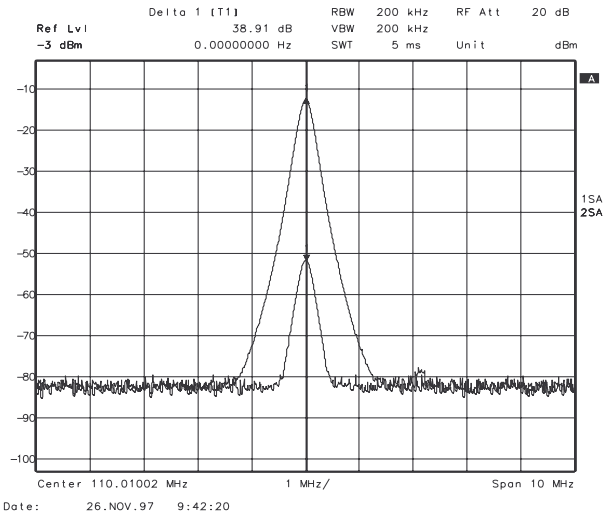

Fig. 4: Measurement of Wanted and Image Signal

This is in good correlation with the simulation results which can be seen in figure [5]. In fact it is possible to get an enormous image rejection of more than 60dB in simulation but this value will never be possible to achieve this value in

mass production because of the spead of capacitors and resitors. Even with worst case parameters of the internal elements it will be no problem to meet the DECT requirements in this point. The powergain of the front end was measured to be higher than 27dB. The overall noise figure is 4.5dB with an IP3 of -23dBm at IC input. The image reject receiver meets the DECT system requirements.

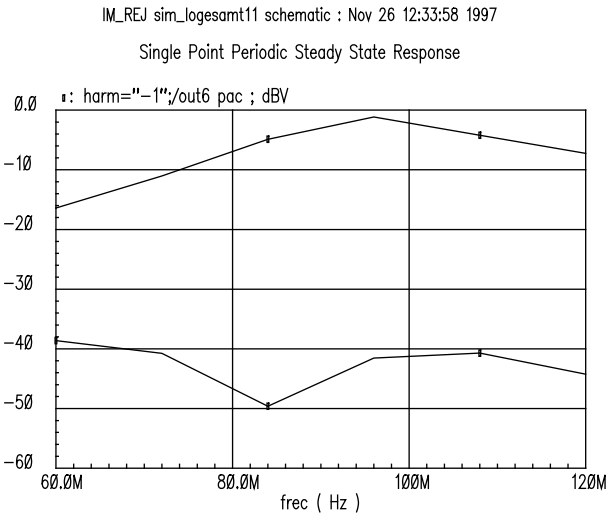

Fig. 5: Simulation of Output Amplitude of Wanted and Image Signal

V. Summary

An image reject receiver IC for DECT was presented. It was shown that the presented realization gives an improvement in overall cost, compared with the 2nd generation receiver. Phase shifter networks were described in detail, advantages and disadvantages have been discussed. The measurement results proof that the complete receiver is fully compatible with the DECT standard.

The disadvantage of the image reject approach is the increased current consumption of the receiver, but for low cost consumer products, such as DECT telephones, the reduction of expensive external components as transistors, filters, and coils is much more important than the current consumption of the analog RX path, because the receiver is only active in 1 of 24 timeslots..

VI. References

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